What Is Claimed Is:

1. A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series; and

a power-down control PMOS transistor; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor across the power and ground levels of said system, wherein said control PMOS transistor is connected at the power end, and said first and second NMOS transistors at the ground end;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as the signal input for said input logic family; the gate terminal of said first PMOS transistor serves as the shifted output of said shifter circuit apparatus; and the gate terminal of said power-down control PMOS transistor is controlled by a power-down control signal to cut off said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

2. The shifter circuit apparatus of claim 1, further comprising a first inverter and a second inverter, wherein said first and second inverters are connected in series, the input of said first inverter is connected to said output, and the output of said

first inverter and the output of said second inverter generate a complementary pair of said shifted output.

3. A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a power-down control PMOS transistor; and

a first inverter and a second inverter; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor across the power and ground levels of said system, wherein said control PMOS transistor is connected at the power end, and said first and second NMOS transistors at the ground end;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as the signal input for said input logic family; the gate terminal of said first PMOS transistor is connected to the input of said first inverter; the output of said first inverter is connected to the input of said second inverter; the output of said second inverter serves as the shifted output of said shifter circuit apparatus; and the gate terminal of said power-down control PMOS transistor is controlled by a power-down control signal to cut off said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

4. The shifter circuit apparatus of claim 3, further comprising a third PMOS transistor, wherein the drain and source terminals of said third NMOS transistor are connected respectively to the input of said first inverter and the ground of said system.

5. The shifter circuit apparatus of claim 3, further comprising a resistor connected across the input of said first inverter and the ground of said system.

6. A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a power-down control PMOS transistor;

a first inverter and a second inverter; and

a third NMOS transistor; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor across the power and ground levels of said system, wherein said control PMOS transistor is connected at the power end, and said first and second NMOS transistors at the ground end;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as the signal input for said input logic family; the gate terminal of said first PMOS transistor is connected to

the input of said first inverter; the output of said first inverter is connected to the input of said second inverter; and the output of said second inverter serves as the shifted output of said shifter circuit apparatus; the drain and source terminals of said third NMOS transistor are connected respectively to the input of said first inverter and the ground of said system; and the gate terminal of said power-down control PMOS transistor is controlled by a power-down control signal to cut off said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

7. The shifter circuit apparatus of claim 1, further comprising a third PMOS transistor connected between the power level of said system and said power-down control PMOS transistor.

8. A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus comprising:

a first transistor pair comprising a first PMOS and a first NMOS transistor connected in series;

a second transistor pair comprising a second PMOS and a second NMOS transistor connected in series;

a third PMOS transistor; and

a power-down control PMOS transistor; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control PMOS transistor and said third PMOS transistor across the power and ground levels of said system, wherein said third PMOS transistor is connected at the power end, and said first and second NMOS transistors at the ground end;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second PMOS transistor, and the node at which the drain terminals of said transistors of said

second transistor pair being connected together is also connected to the gate of said first PMOS transistor; and

the gate terminal of said first NMOS transistor serves as the signal input for said input logic family; the gate terminal of said first PMOS transistor serves as the shifted output of said shifter circuit apparatus; and the gate terminal of said power-down control PMOS transistor is controlled by a power-down control signal to cut off said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition.

9. The shifter circuit apparatus of claim 8, wherein said third PMOS transistor is a constant current source.

10. A dynamic CMOS level shifter circuit apparatus in a digital electronic system for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level for a second logic family, said shifter circuit apparatus comprising:

a first transistor pair comprising a first NMOS and a first PMOS transistor connected in series;

a second transistor pair comprising a second NMOS and a second PMOS transistor connected in series; and

a power-down control NMOS transistor; wherein:

said first and second transistor pairs are connected in parallel, and said parallel connection is connected in series with said power-down control NMOS transistor across the power and ground levels of said system, wherein said control NMOS transistor is connected at the power end, and said first and second PMOS transistors at the ground end;

the node at which the drain terminals of said transistors of said first transistor pair being connected together is also connected to the gate of said second NMOS transistor, and the node at which the drain terminals of said transistors of said second transistor pair being connected together is also connected to the gate of said first NMOS transistor; and

the gate terminal of said first PMOS transistor serves as the signal input for said input logic family; the gate terminal of said first NMOS transistor serves as the shifted output of said shifter circuit apparatus; and the gate terminal of said power-down control NMOS transistor is controlled by a power-down control signal to cut off said first and second NMOS transistors for a duration of time sufficient for said first and second PMOS transistors to settle state transition.